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Attention: Examiner: Juan A. Torres
Supervisory Examiner: Mohammad H. Ghayour
UNITED STATES PATENT AND TRADEMARK OFFICE
Mail Stop Appeal Brief-Patents

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Date: January 23, 2006

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CERTIFICATION OF FACSIMILE TRANSMISSION UNDER 37 CFR 1.8

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Georgann S. Grunebach, Reg. No. 33,179
(Printed Name of Depositor)

January 23, 2006
(Date of Signature)

Attention: Commissioner for Patents

Attorney Docket No. PD-201148

Please find attached Re:

Serial No.: ~~10/408,898~~ 10/068,039

Filing Date: April 8, 2003

>TRANSMITTAL LETTER FOR APPEAL BRIEF IN DUPLICATE (2 pages)

>APPEAL BRIEF INCLUDING APPENDIX (17 pages)

>Resubmission of Amendment Under §1.116 (6 pages)

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PATENT
Docket No. PD-201148
CUSTOMER NO.: 020991

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Ernest C. Chen, et al.	:	Date: January 23, 2006
Serial No.:	10/068,039	:	Group Art Unit: 2631
Filed:	February 5, 2002	:	Examiner: Juan A. Torres

For: PREPROCESSING SIGNAL LAYERS IN LAYERED MODULATION DIGITAL SIGNAL SYSTEM TO USE LEGACY RECEIVERS

TRANSMITTAL LETTER FOR APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir: Transmitted herewith is an Appeal Brief in the above-identified application.

_X_ The Appeal Brief Fee of $500.00 is due.

Charge **$ 500.00** to Deposit Account No. 50-0383 of The DIRECTV Group, Inc. (formally Hughes Electronics Corporation), El Segundo, California. Please charge any additional fees for claims or credit overpayment to Deposit Account No. 50-0383. If any additional extension fee is required, please charge to Deposit Account No. 50-0383. **This form is submitted in duplicate.**

Respectfully submitted,

Georgann S. Grunebach, Reg. No.: 33,179
Attorney for Appellants

Certification of Facsimile Transmission UNDER 37 CFR 1.8

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Georgann S. Grunebach, Reg. No.: 33,179
Attorney for Appellant

January 23, 2006
Date

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Georgann S. Grunebach, Reg. No. 33,179

Customer No. 020991

Due Date: January 23, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	
Inventor: Ernest C. Chen et al.	Examiner: Juan A Torres
Serial #: 10/068,039	Group Art Unit: 2631
Filed: February 5, 2002	Appeal No.: ______
Title: PREPROCESSING SIGNAL LAYERS IN LAYERED MODULATION DIGITAL SIGNAL SYSTEM TO USE LEGACY RECEIVERS	

BRIEF OF APPELLANTS

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR §1.192, Appellants hereby submit the Appellants' Brief on Appeal from the final rejection in the above-identified application, as set forth in the Office Action dated August 26, 2005.

Please charge the amount of $500.00 to cover the required fee for filing this Appeal Brief as set forth under 37 CFR §1.17(c) to Deposit Account No. 50-0383 of The DIRECTV Group, Inc., the assignee of the present application. Also, please charge any additional fees or credit any overpayments to Deposit Account No. 50-0383.

01/26/2006 EFLORES 00000006 500383 10068039
01 FC:1402 500.00 DA

I. REAL PARTY IN INTEREST

The real party in interest is The DIRECTV Group, Inc., the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for the above-referenced patent application.

III. STATUS OF CLAIMS

Claims 31-39 are pending in the application.

Claims 31-39 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,039,961 to Ishio (hereinafter, Ishio) and further in view of U.S. Patent No. 6,297,691 to Anderson (hereinafter, Anderson).

Claims 35 and 38 are rejected as depending on a rejected base claim, but are indicated as allowable if rewritten in independent form to include the base claim and any intervening claims.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Office Action, the Applicants attempted to cancel claims 1-30 and to amend claims 33 and 39. The Examiner refused entry of the amendments because they would "further consideration and/or search," and did not indicate if the cancellation of claims 1-30 would be entered. To resolve the issue, the Applicants concurrently submit an amendment under 37 C.F.R. § 1.116, canceling claims 1-30.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In an embodiment related to claim 31, the Applicants' invention is evidenced by an apparatus for receiving a non-coherent layered modulation signal comprised of a sum of a first layer signal and a second layer signal. The apparatus comprises a tuner (item 500 of FIG. 5 and discussed in paragraph [0036] of the Applicants' specification) for receiving the non-coherent layered modulation signal and producing a layered in-phase signal and a layered quadrature signal; an analog-to-digital converter (item 504 of FIG. 5 and discussed in paragraph [0036] of the Applicants'

specification) for digitizing the layered in-phase signal and the layered quadrature signal, and a processor (item 506 of FIG. 5 and discussed in paragraphs [0036]-[0040]) for processing the digitized layered in-phase signal and the digitized layered quadrature signal to produce a lower layer in-phase signal and a lower layer quadrature signal, an upper layer in-phase signal and an upper layer quadrature signal.

The processor comprises a modulation map (item 520-522 of FIG. 5 and discussed in paragraph [0038]) configured to modify the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal, and a subtractor (item 538 of FIG. 5 and discussed in paragraph [0039] of the specification) configured to subtract the ideal upper layer in-phase signal from the digitized layered in-phase signal to produce the lower layer in-phase signal and to subtract the ideal upper layer quadrature signal from the digitized layered quadrature signal to produce the lower layer quadrature signal.

The apparatus also comprises a digital-to-analog converter (item 540 of FIG. 5 and discussed in paragraph [0040] of the specification) for converting the lower layer in-phase signal and the lower layer quadrature signal to a lower layer in-phase analog signal and a lower layer quadrature analog signal, and a modulator (item 544 of FIG. 5 and discussed in paragraph [0040] of the Applicants' specification) for modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal.

In an embodiment related to claim 36, the Applicants' invention is evidenced by a method of receiving a non-coherent layered modulation signal comprised of a sum of a first layer signal and a second layer signal. The method comprises the steps of receiving the layered modulation signal and producing a layered in-phase signal and a layered quadrature signal (discussed in paragraph [0041]), digitizing the layered in-phase signal and the layered quadrature signal (discussed in paragraph [0041]), decoding the layered in-phase signal and the layered quadrature signal to produce a lower layer in-phase signal (discussed in paragraph [0041]), a lower layer quadrature signal, an upper layer in-phase signal and an upper layer quadrature signal. The decoding step comprises the steps of modifying the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to

produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal (discussed in paragraph [0038]), subtracting the ideal upper layer in-phase signal from the layered in-phase signal to produce the lower layer in-phase signal (discussed in paragraph [0039]), subtracting the ideal upper layer quadrature signal from the layered quadrature signal to produce the lower layer quadrature signal (discussed in paragraph [0039]); converting the lower layer in-phase signal and the lower layer quadrature signal to a lower layer in-phase analog signal and a lower layer quadrature analog signal (discussed in paragraph [0040]); and modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal (discussed in paragraph [0040]).

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Whether claims 31-39 are patentable under 35 U.S.C. § 103(a) over U.S. Patent No. 4,039,961, issued to Ishio (hereinafter, the Ishio reference) and further in view of U.S. Patent No. 6,297,691 to Anderson (hereinafter, the Anderson reference).

VII. ARGUMENTS

A. Claims 31-39 are patentable under 35 U.S.C. § 103(a) over Ishio in view of Anderson

1. The Ishio Reference

Ishio discloses a digital carrier signal demodulation circuit that is used in the carrier digital transmission system utilizing a 16-ary APK (Amplitude and Phase Keying) signal produced by the vector superposition of a second path signal consisting of a four-phase shift keying signal upon each phase of a first path signal consisting of a four-phase shift keying signal, the level of the second path signal being lower than that of the first path signal. The received 16-ary APK signal is detected with the reference carrier extracted from the received signal, regenerated to reproduce the base band pulses of the first path signal. The recovered base band pulses remodulate the reference carrier to produce the first path signal. The phases of the recovered first path signal and received signal are compared to phase lock a voltage controlled oscillator thereby producing the reference character.

2. The Anderson Reference

Anderson discloses a receiver receives modulated message signals in non-coherent FSK and coherent 8PSK protocols. A selectively configurable processor demodulates the message signals, and includes a demodulator that derives in-phase and quadrature signals based on the message signals. A phase detector is responsive to the in-phase and quadrature signals and delayed in-phase and quadrature signals to derive a phase signal. A selector is responsive to the in-phase and quadrature signals to selectively connect a loop filter between the phase detector and the demodulator. When the selector connects the filter between the phase detector and demodulator, the demodulator is responsive to filtered phase signals to lock onto a frequency of the message signals so that the processor operates as a phase locked loop to demodulate coherent modulated signals. When the selector disconnects the filter from between the phase detector and the demodulator, the demodulator demodulates non-coherent modulated signals and the phase detector supplies a phase signal representing the slope of the phase of the demodulated signal.

3. Independent Claim 31 is Patentable over Ishio in view of Anderson

Claim 31 recites:

> *An apparatus for receiving a non-coherent layered modulation signal comprised of a sum of a first layer signal and a second layer signal, the apparatus comprising:*
>
> *a tuner for receiving the non-coherent layered modulation signal and producing a layered in-phase signal and a layered quadrature signal;*
>
> *an analog-to-digital converter for digitizing the layered in-phase signal and the layered quadrature signal;*
>
> *a processor for processing the digitized layered in-phase signal and the digitized layered quadrature signal to produce a lower layer in-phase signal and a lower layer quadrature signal, an upper layer in-phase signal and an upper layer quadrature signal, the processor comprising:*
>
> > *a modulation map configured to modify the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal; and*
> >
> > *a subtractor configured to subtract the ideal upper layer in-phase signal from the digitized layered in-phase signal to produce the lower layer in-phase signal and to subtract the ideal upper layer quadrature signal from the digitized layered quadrature signal to produce the lower layer quadrature signal;*
>
> *a digital-to-analog converter for converting the lower layer in-phase signal and the lower layer quadrature signal to a lower layer in-phase analog signal and a lower layer quadrature analog signal; and*
>
> *a modulator for modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal.*

a) Even when Combined, Ishio and Anderson Do Not Teach All of the Features of Claim 31

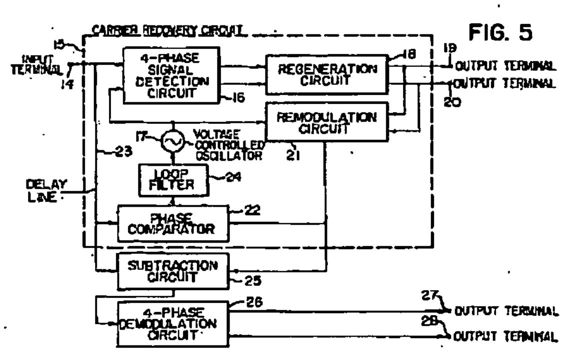
(1) Ishio and Anderson Both Fail to Teach a Modulation Map

Claim 31 recites "a modulation map, configured to modify the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal." According to the Final Office Action, this is disclosed by the "Remodulation Circuit 21" shown in FIG. 5 below and in the associated text:

FIRST EMBODIMENT, FIG. 5

Referring to FIG. 5, the first embodiment of a demodulation circuit in accordance with the present invention will be described. The input 16-ary APK signal is applied from an input terminal 14 to a four-phase signal detection circuit 16 in a carrier recovery circuit 15 (a block indicated by the dotted lines) to be coherently detected with the reference carriers of the X-and Y-axes phase shown in FIG. 4 which is produced by a voltage controlled oscillator 17. The detected output is discriminated by a regeneration circuit 18 in order to detect the quadrant in which the signal vector is present (See FIG. 4), and the outputs derived from output terminals 19 and 20 correspond to the base band pulses applied to the input terminals ch1 and ch2 shown in FIG. 3.

FIG. 5



The outputs from the regeneration circuit 18 are also applied to a re-modulation circuit 21 in order to modulate the reference carrier from the oscillator 17 into the four-phase modulated signal corresponding to the signal vector indicated by the solid line segment in FIG. 4. That is, the first path signal is regenerated. The first path signal is applied to a phase comparator 22, to which is also applied the input signal which has been delayed by a delay line 23 by a time equal to the signal transmission delay time from the input terminal to the output of the re-modulation circuit 21. The output from the phase comparator 22 which compares the phase between the first pulse signal and the input signal from the input terminal 14, is applied through a loop filter 24 to the oscillator 17 as the control voltage. Since one of the two input signals applied to the phase comparator 22 is the first path signal while the other, the resultant or sum signal of the addition of the first and second path signal vectors, their amplitudes and phases are not exactly coincident, but the second path signal may be considered as an interference signal to the first path signal so that when the difference in level between the first and second path signals is suitably selected, the satisfactory operation of the loop controlling the oscillator 17 may be ensured.

The output from the re-modulation circuit 21 is also applied to a subtraction circuit 25 where it is vectorially subtracted from the input signal from the input terminal 14. The output from the subtraction circuit 25 is the second path signal corresponding to the signal vector indicated by the dotted line segment in FIG. 4. The second path signal is applied to a four-phase demodulation circuit 26 so that the four-phase PSK signal corresponding to the base band pulses applied to the input terminals ch3 and ch4 (see FIG. 3) may be derived from output terminals 27 and 28.

The Applicants respectfully disagreed. The foregoing discloses is a "remodulation circuit 21" that remodulates the signal present at the output terminals (19, 20). No mention is made of

anything analogous to any element that *modifies the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal*, let alone a *modulation map*. It's absence is plain from inspection.

In the telephonic interview held October 25, 2005, it was suggested that a modulation map may be inherent to the Ishio disclosure. If that is the nature of the rejection, the Applicants respectfully disagree.

Inherency "may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1269 (Fed. Cir. 1991). Instead, to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co.*, 948 F.2d at 1268.

Nothing in any of the cited references justifies a conclusion that a "modulation map for modifying the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal" is *necessarily present* in the Ishio reference. Nor would one of ordinary skill in the art consider it to be necessary. There are many ways by which signal transmission errors can be accounted for, including (1) signal coding, as described in col. 3, line 28 - col. 4, line 4 of U.S. Patent 5,966,412 (considered by the Examiner on March 29, 2005) and (2) predistortion of the transmitted signal, as described in "Adaptive Linearization of Power Amplifiers in Digital Radio Systems," by Saleh et al. (also considered by the Examiner on March 29, 2005).

In the Advisory Action mailed November 10, 2005, the Examiner argued that Figs 2, 8, 9, and 13 of the Ishio reference also show modulation mapping, and further argued:

> "If block 21 is not able to know the mapping will not be able to remodulate the signal. The re-modulator 21 will eliminate channel noise from the upper layer signal, mapping the received point to the most probable point in the transmitter constellation. For these reasons and the reason stated in the previous Office action, the rejection of claims 31 and 36 are maintained."

This is simply a refomulation of the "inherency" argument above. The use of "a modulation map configured to modify the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal" is not disclosed or inherent to Ishio's remodulator.

The Advisory Action also asserts that Ishio shows a more complex mapping with 3 bits in Figs. 17 and 18. However, this is not "a modulation map configured to modify the upper layer in-phase signal and the upper layer quadrature signal to produce an ideal upper layer in-phase signal and a ideal upper layer quadrature signal," as recited in claim 31.

Although the Office Actions do not reject claim 31 on the basis that it would be obvious to modify Ishio and Anderson the Applicants point out that such a rejection would be improper as well for the same reasons. Further, even if transmission distortions were not sufficiently ameliorated by coding schemes or better handled via the transmitted signal as taught by Saleh (and no evidence has been presented that this is the case), the question remains as to why one of ordinary skill in the art would have modified the *reconstructed* upper layer signal rather than modifying the received signal *before* demodulation, and subtracting the remodulated signal from that modified received signal, and also why a modulation *map* would be used. To maintain a prima facie rejection under 35 U.S.C. § 103, there must not only be some teaching to modify the references not only to do what the Applicants have done, but in *how* they have done it, because how they have done it is recited in the claim itself.

(2) Ishio and Anderson Both Fail to Teach and A/D Converter Digitizing Layered In Phase Signal and Layered Quadrature Signal

The Final Office Action indicated that the Applicants' " *analog-to-digital converter for digitizing the layered in-phase signal and the layered quadrature signal* is disclosed by block 18 of FIG. 5 above and in column 4, lines 3-52 of the Ishio reference (both reproduced above). The Applicants respectfully disagree, as the reference does mention an A/D converter.

The Advisory Action argued that the A/D converter is shown in block 16 of FIG. 5. Visual inspection reveals that it is a 4 phase signal detection circuit, not an A/D converter. The Advisory Action also argues that block 14 of FIG. 3 discloses an A/D converter for digitizing the layered in-phase signal and the layered quadrature signal. Inspection again reveals that this is not the case.

(3) Ishio and Anderson Both Fail to Teach a Modulator for Modulating the Lower Layer Analog Signal and the Lower Layer Quadrature Signal

The Final Office Action indicated that the Applicants' *modulator for modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal*' is disclosed by the "remodulation circuit 21" of the Ishio reference.

While it is true that block 21 discloses a "remodulator", which modulates an input signal, it does not modulate *the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal* as recited in claim 31 ... it remodulates the upper layer signal. It is difficult to see how the "remodulation circuit 21" could reasonably be said to disclose both the "modulation map" that provides the ideal upper layer signal and modulated lower layer signals as well.

b) There is no Teaching to Modify Ishio as Taught by Anderson

The First Office Action suggested that the motivation to modify Ishio was to "demodulate coherence and non-coherence signals reducing the cost of the decoder and to have compatibility with other systems" to offer compatibility with other systems.

However, communications systems engineers do not typically design receivers to include features that are not wanted or needed just for purposes of compatibility with other systems, unless there is some suggestion that the benefits of such compatibility outweigh the additional cost and complexity.

The Final Office Action further argued that

> "The coherent and non-coherent of a signal is independent of the use of layered modulation. Ishio presents a case of coherent signals for simplification, but the coherent of the signals is not important in his patent, in fact he only mentions that one time. Ishio never discloses that his invention is not applicable to non-coherent signals."

The Applicants answer each statement as follows:

<u>The Coherence and Non-Coherence of a Signal is Independent of the Use of Layered Modulation</u>: This appears to be either (a) argues that is *possible* to receive a layered modulation signal having non-coherent layers, or (b) argues that it is well known to receive a layered modulation signal having non-coherent layers.

If (a) applies, the statement is not relevant to the issue of whether the Applicants' claims are patentable over the prior art. It is, of course, possible to do so, or the Applicants' invention would lack utility under 35 U.S.C. § 101.

If (b) applies, the Applicants respectfully traverse, and in accordance with MPEP 2144.03, request that the Examiner produce evidence supporting this contention. Prior to conception of their invention, the Applicants know of no system that receives a layered modulation signal having two non-coherently layered signals (an upper layer signal non coherently layered with a lower layer signal) to produce both the received upper and lower layer signals.

<u>Ishio Presents a Case of Coherent Signals for Simplification, but the Coherence of the Signals is Unimportant</u>: The Applicants' respectfully suggest that this is a statement made in hindsight, and hindsight is impermissible in determining the Applicants' claims. The Applicants also disagree that the coherency of the signals is a mere "simplification" or that it is "unimportant" to Ishio.

<u>Ishio Never Discloses that His Invention is Not Applicable to Non-Coherent Signals</u>: This, of course, is not the law of obviousness.

4. Independent Claim 36 is Patentable over Ishio in view of Anderson

The Applicants respectfully traverse the rejection of claim 36 for the same reasons as claim 31.

5. Dependent Claims 32-35 and 37-39 are Patentable over Ishio in View of Anderson

Dependent claims 32-35 and 37-39 recite the features of the claims they depend upon, and are patentable for the same reasons.

VIII. CONCLUSION

In light of the above arguments, Appellants respectfully submit that the cited references do not anticipate nor render obvious the claimed invention. More specifically, Appellants' claims recite novel physical features which patentably distinguish over any and all references under 35 U.S.C. §§ 102 and 103. As a result, a decision by the Board of Patent Appeals and Interferences reversing the Examiner and directing allowance of the pending claims in the subject application is respectfully solicited.

Respectfully submitted,

Date: January 23, 2006

By: ____________________
Name: Georgann S. Grunebach
Registration No.: 33,179

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CLAIMS APPENDIX

1. - 30. (CANCELED)

31. (PREVIOUSLY PRESENTED) An apparatus for receiving a non-coherent layered modulation signal comprised of a sum of a first layer signal and a second layer signal, the apparatus comprising:

a tuner for receiving the non-coherent layered modulation signal and producing a layered in-phase signal and a layered quadrature signal;

an analog-to-digital converter for digitizing the layered in-phase signal and the layered quadrature signal;

a processor for processing the digitized layered in-phase signal and the digitized layered quadrature signal to produce a lower layer in-phase signal and a lower layer quadrature signal, an upper layer in-phase signal and an upper layer quadrature signal, the processor comprising:

a modulation map configured to modify the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal; and

a subtractor configured to subtract the ideal upper layer in-phase signal from the digitized layered in-phase signal to produce the lower layer in-phase signal and to subtract the ideal upper layer quadrature signal from the digitized layered quadrature signal to produce the lower layer quadrature signal;

a digital-to-analog converter for converting the lower layer in-phase signal and the lower layer quadrature signal to a lower layer in-phase analog signal and a lower layer quadrature analog signal; and

a modulator for modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal.

32. (PREVIOUSLY PRESENTED) The apparatus of Claim 31, wherein the processor is adapted to produce the layered in-phase signal and the layered quadrature signal by match filtering the layered in-phase signal and the layered quadrature signal.

33. (PREVIOUSLY PRESENTED) The apparatus of claim 31, wherein the lower layer signal is a legacy signal.

34. (PREVIOUSLY PRESENTED) The apparatus of Claim 31, wherein the processor is further configured to delay the digitized layered in-phase signal and the digitized layered quadrature signal to synchronize the subtraction of the ideal upper layer in-phase signal from the layered in-phase signal and the subtraction of the ideal upper layer in-phase signal from the layered in-phase signal.

35. (PREVIOUSLY PRESENTED) The apparatus of claim 34, wherein the processor further comprises:

a first delay element configured to apply a first delay to the digitized layered in-phase signal and the digitized layered quadrature signal;

an amplitude and phase matching coefficient generator, configured to generate amplitude and phase matching coefficients from the digitized and first delayed layered in-phase signal, the digitized and first delayed quadrature signal, the modified upper layer in-phase signal and the modified upper layer quadrature signal;

an amplitude and phase matcher configured to apply the amplitude and phase matching coefficients to the modified upper layer in-phase signal and the modified upper layer quadrature signal to generate the ideal upper layer in-phase signal and the ideal upper layer quadrature signal; and

a second delay element, configured to apply a second delay to the digitized and first delayed layered in-phase signal and the digitized and first delayed layered quadrature signal to produce the delayed digitized layered in-phase signal and the delayed digitized layered quadrature signal.

36. (PREVIOUSLY PRESENTED) A method of receiving a non-coherent layered modulation signal comprised of a sum of a first layer signal and a second layer signal, the method comprising the steps of:

receiving the layered modulation signal and producing a layered in-phase signal and a layered quadrature signal;

digitizing the layered in-phase signal and the layered quadrature signal;

decoding the layered in-phase signal and the layered quadrature signal to produce a lower layer in-phase signal, a lower layer quadrature signal, an upper layer in-phase signal and an upper layer quadrature signal, comprising the steps of:

modifying the upper layer in-phase signal and the upper layer quadrature signal to account for transmission distortions of the layered modulation signal to produce an ideal upper layer in-phase signal and an ideal upper layer quadrature signal;

subtracting the ideal upper layer in-phase signal from the layered in-phase signal to produce the lower layer in-phase signal;

subtracting the ideal upper layer quadrature signal from the layered quadrature signal to produce the lower layer quadrature signal;

converting the lower layer in-phase signal and the lower layer quadrature signal to a lower layer in-phase analog signal and a lower layer quadrature analog signal; and

modulating the lower layer in-phase analog signal and the lower layer quadrature analog signal to produce a single layer signal.

37. (PREVIOUSLY PRESENTED) The method of Claim 36, wherein the step of decoding further comprises delaying the digitized layered in-phase signal and the digitized layered quadrature signal to synchronize the subtraction of the ideal upper layer in-phase signal from the layered in-phase signal and the subtraction of the ideal upper layer in-phase signal from the layered in-phase signal.

38. (PREVIOUSLY PRESENTED) The method of claim 37, wherein the step of decoding the layered in-phase signal and the layered quadrature signal comprises the steps of:

applying a first delay to a the digitized layered in-phase signal and the digitized layered quadrature signal;

generating amplitude and phase matching coefficients from the digitized and first delayed layered in-phase signal, the digitized and first delayed quadrature signal, the modified upper layer in-phase signal and the modified upper layer quadrature signal;

applying the amplitude and phase matching coefficients to the modified upper layer in-phase signal and the modified upper layer quadrature signal to generate the ideal upper layer in-phase signal and the ideal upper layer quadrature signal;

applying a second delay to the digitized and first delayed layered in-phase signal and the digitized and first delayed layered quadrature signal to produce the delayed digitized layered in-phase signal and the delayed digitized layered quadrature signal.

39. (PREVIOUSLY PRESENTED) The method of claim 36, wherein the lower layer signal is a legacy signal.

EVIDENCE APPENDIX

(none)

RELATED PROCEEDINGS APPENDIX

(none)